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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,967	11/27/2001	Takashi Yamada	P 28403201F171	8085

7590 07/17/2002

PILLSBURY WINTHROP LLP
1600 TYRONS BOULEVARD
MCLEAN, VA 22102

EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,967	YAMADA ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the application filed November 27, 2001.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8, drawn to a semiconductor structure with DRAM cells, classified in class 257, subclass 71.

II. Claims 9-20, drawn to the method for manufacturing a semiconductor structure with DRAM cells, classified in class 438, subclass 296.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

A telephone conversation took place with Dale Lazar on June 18, 2002 which resulted in a provisional election being made without traverse to prosecute the semiconductor structure with DRAM cells, claims 1-8. Affirmation of this election must be made by applicant in replying to this Office action. Claims 9-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "width-increased groove portion" (See Claims 1 and 3-5); b) "island-like" (See Claims 6-8); c) "continuously disposed along one direction and also with a bit line coupled to the second diffusion layer of said transistor being provided to cross said word line" (See Claim 6); and d) "bit line is in contact with said second diffusion layer per each DRAM cell" (See Claim 7). Claim 2 depends directly or indirectly from a rejected claim and is, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, as far as understood, are rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Womack et al. (U.S. Patent No. 4,713,678).

In regards to claim 1, Lee discloses the following:

a) an element substrate (10) including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate (26) with a dielectric film (20) interposed there between (See Figure 2);

b) element substrate having a groove, said groove being formed to have a width-increased groove portion in said dielectric film (See Figure 2 and 14);

c) an impurity diffusion source buried in said width increased groove portion of said groove to be contacted with said bottom surface of said semiconductor layer; and

d) a transistor having a first diffusion layer (32) of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer (34) of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode (34) formed at a side face of said groove over said impurity diffusion source with a gate insulation film (36) between said side face and said gate electrode (See Figure 2 and 14).

In regards to claim 1, Lee fails to disclose the following:

a) groove with a depth extending from a top surface of said semiconductor layer into said dielectric film.

However, Womcak et al. ("Womack") discloses a groove that extends into the substrate (See Figure 4a). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a groove that had a large depth as disclosed in Womack because it aids in enhancing the storage capacitor area.

In regards to claim 2, Lee discloses the following:

a) a trench capacitor (16) (See Figure 2); and

b) storage electrode (18) (See Figure 2).

In regards to claim 2, Barber fails to disclose the following:

a) groove is formed deep enough to reach the inside of said semiconductor substrate after penetration through said dielectric film.

However, Womack discloses a groove that extends into the substrate (See Figure 4a). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a groove that had a large depth as disclosed in Womack because it aids in enhancing the storage capacitor area.

8. Claim 3, as far as understood, is rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Womack et al. (U.S. Patent No. 4,713,678) and Applicant's Prior Art Drawing.

In regards to claim 3, Barber fails to disclose the following:

a) a buried strap for use as said impurity diffusion source is formed and buried in said width-increased groove portion overlying said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof, and wherein this buried strap is covered with a cap insulation film with the gate electrode of said transistor embedded to overlie said cap insulation film.

However, Applicant's Prior Art Drawing discloses a strap (3) buried in a groove (See Figure 37). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a strap as disclosed in Applicant's Prior Art Drawing because it aids in moving one material through another.

9. Claims 6-8, as far as understood, are rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Womack et al. (U.S. Patent No. 4,713,678) and Hieda et al. (U.S. Patent No. 5,508,541).

In regards to claim 6, Barber discloses the following:

a) a word line connected to the gate electrode (34) of said transistor being continuously disposed along one direction and also with a bit line (44) coupled to the second diffusion layer of said transistor being provided to cross said word line (See Figure 2).

In regards to claim 6, Barber fails to disclose the following:

a) semiconductor layer is partitioned into a plurality of island-like element regions by an element isolating insulative film as formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said island like element region.

However, Hieda et al. ("Hieda") discloses a semiconductor layer divided into multiple regions (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Barber to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

In regards to claim 7, Barber discloses the following:

a) bit line is in contact with said second diffusion layer per each DRAM cell at a position adjacent to word lines (See Figure 2).

In regards to claim 7, Barber fails to disclose the following:

a) island-like element region.

However, Hieda discloses a semiconductor layer divided into multiple regions (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Barber to include a semiconductor

layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

b) a body wire lead is formed to be contacted with said semiconductor layer across central part of said island-like element region for applying a fixed potential to said semiconductor layer.

However, Hieda discloses a polysilicon layer (60) (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Barber to include a polysilicon layer as disclosed in Hieda because it aids in providing a connection among the various components.

In regards to claim 8, Barber discloses the following:

a) a word line connected to the gate electrode of said transistor being continuously disposed along one direction and also with a bit line coupled to the second diffusion layer of said transistor being provided to cross said word line (See Figure 2).

In regards to claim 8, Barber fails to disclose the following:

a) semiconductor layer is partitioned into a plurality of island-like element regions by an element isolating insulative film as formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said island like element region.

However, Hieda discloses a semiconductor layer divided into multiple regions (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Barber to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

Allowable Subject Matter

10. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Uchida (U.S. Patent No. 4,792,834) discloses a memory device with a buried layer; b) Hwang et al. (U.S. Patent No. 4,833,516) discloses a high density memory cell structure; c) Beilstein, Jr. et al. (U.S. Patent No. 5,055,898) discloses a DRAM memory cell; d) Chatterjee et al. (U.S. Patent No. 5,208,657) discloses a DRAM cell with a trench capacitor; f) Matsuo et al. (U.S. Patent No. 5,316,962) discloses a semiconductor device that has trench capacitors; g) Tadaki et al. (U.S. Patent No. 5,349,218) discloses a device including memory cells; h) Yamada et al. (U.S. Patent No. 5,502,320) discloses a DRAM device; i) Noble, Jr. (U.S. Patent No. 5,512,767) discloses a trench capacitor; j) Nitayama et al. (U.S. Patent No. 5,905,279) discloses a low resistant trench; k) Schrems et al. (U.S. Patent No. 5,945,704) discloses a trench capacitor with a buried layer; l) Wada (U.S. Patent No. 5,998,822) discloses an integrated circuit; and m) Parekh et al. (U.S. Patent No. 6,005,268) discloses DRAM cells and capacitors.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

July 5, 2002

Carl Whitehead Jr.

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800